AC5713A Datasheet

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AC5713A Features

CPU Core

- Dual-core 32-bit CPU
- 32KB I-Cache
- 24KB D-Cache
- 96K On-chip SRAM
- The maximum operating frequency is 240MHz
- Peripherals can access external memory through cache
- Support IEEE-754 standard single-precision floating point

Interrupts

- 256 interrupt sources with 8 levels of programmable priority
- Support external I/O interrupt
- With soft interrupt (virtual interrupt) function, priority can be configured

Video Codec

- H.264 codec, encoding maximum support:
  - Single mode: 1920×1080@60fps
  - Dual mode: 1920×1080@30fps + 1280×720@30fps
- M-JPEG codec

Image Signal Processor

- Support maximum size: 2304×1296
- Support 8-bit / 10-bit / 12-bit RAW data
- Support 16-bit YUV / 24-bit RGB data
- Support RGBIR sensor
- Support AE / AWB
- Support WDR technology
- Support advanced color enhance
- Support 2D/3D noise reduction
- Support sharpness process
- Support video scaling and digital zoom
- Support video deinterlacing
- Support real time recording OSD
- Support true color logo OSD

Display Processor

- Supports image brightness, contrast, and saturation adjustments
- Supports multiple image layer output (can achieve picture-in-picture)
- Support multiple OSD graphics overlay
- Support image horizontal and vertical mirroring
- Support 90/180/270 degree image rotation
- Support maximum resolution 1920×1080

Video input interface

- One high-speed composite parallel data interface
  - Support 8-bit data width
  - Support BT656 / BT1120 timing
  - Support single / dual / quad channel composite data
  - Support maximum frequency 148.5MHz DDR
- One MIPI CSI interface
  - Support 8-bit / 10-bit / 12-bit RAW data
  - Support 16-bit YUV / 24-bit RGB data
  - Support 1/2lane mode
  - Support DSI mode

Video output interface

- One parallel data interface
  - Support 3 / 6 / 8bit data width
  - Support DVP / BT601 / BT656 / BT1120(16-bit mode) timing
  - Support YUV444 / YUV422 / RGB / RGB565 data formats
- One MIPI DSI interface
  - Support 16-bit / 18-bit / 24-bit data width
  - Support RGB / RGB565 data format
  - Support sync pulse mode / sync event mode / burst mode
  - Support DCS mode
- One AVOUT interface
  - Support NTSC / PAL formats
  - Support 960H format

Audio codec

- 2 PGA for MIC in
- 2 channels delta-sigma audio ADC with SNR > 85 dB
- 2 channels delta-sigma audio DAC with SNR > 95 dB
- Support 8/11.025/12/16/22.05/24/32/44.1/48KHz Sample Rate

Peripheral interface

- Peripheral pin select function
- Up to 49 programmable digital I/O pins
- Support 5 IO port wake-up MCU
- Support peripheral wake-up MCU
- 5 32-bit reloadable timers for timing / capture and PWM
- 3 SPI host controllers, support DMA
- 3 SDIO 2.0 interfaces, support DMA
- 2 I^2C controllers, support master and slave modes
- 4 UARTs, 2 of which support DMA loop buffer
- 8 channels motor PWM

- EMI controller (8-bits), support DMA send
- 1 high speed USB SIE, support HUB
- RTC, with alarm clock and time base to wake up the chip
- Support programable pipeline DMA copy
- Watchdog
- CRC check

Memory Interface

- DDRX controller, support DDR1
  - 16-bit data width
  - Support DDR1@400MHz
  - Maximum support 32×16Mbit
- 1 high-speed SPI flash interface
  - Support standard, dual and quad modes
  - Maximum support 16MB, 80MHz

Analog Peripheral Features

- 2 clock oscillation circuits
- One high speed USB 2.0 PHY
- 4 clock generators (PLLs), provide various system frequencies
- 8 channels 10-bit key general ADC
- 3 lanes MIPI CSI PHY
- 8-level low voltage detector
- Power-on reset

Package type

- AC5713A4: 16×16Mbit/DDR1
- QFN88(10mm×10mm)

1. Pin Defintion

1.1 Pin Assignment

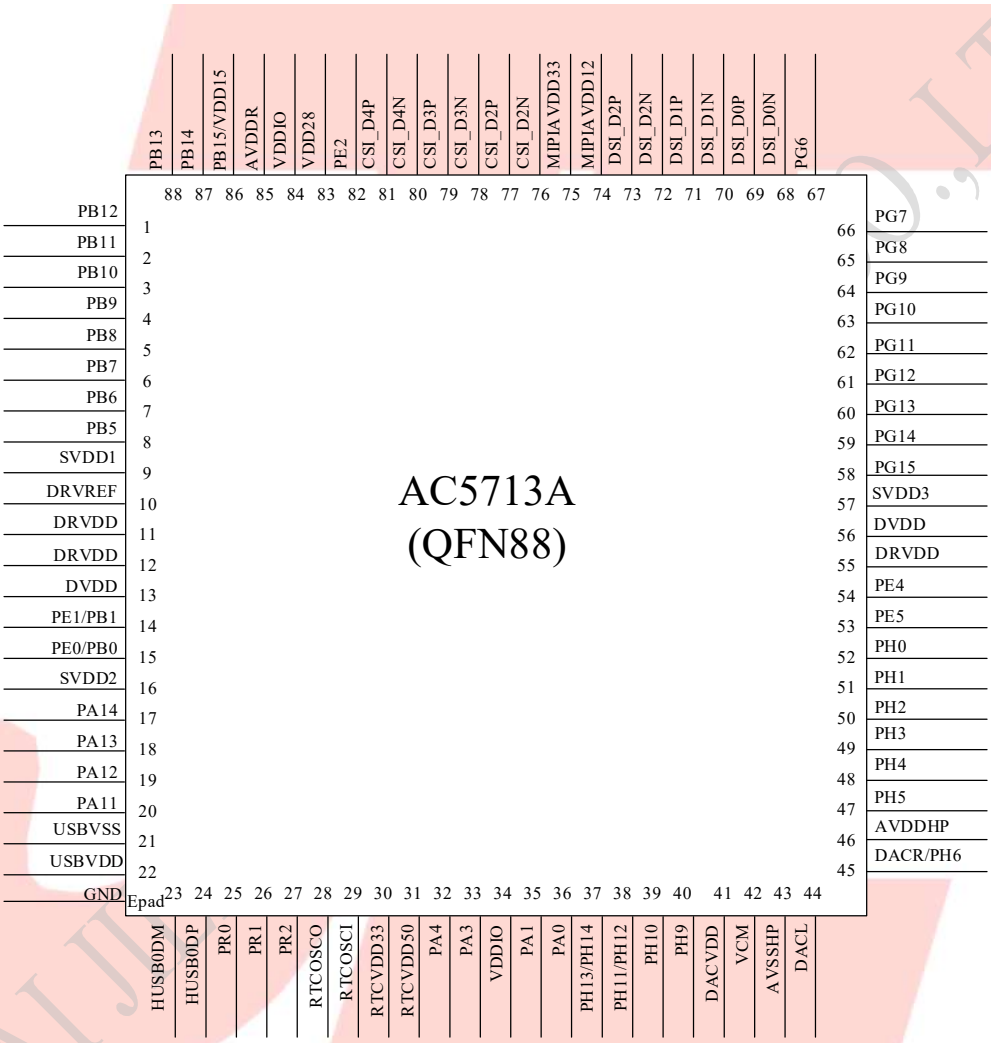


Figure 1-1 AC5713A_QFN88 Pin Assignment

★Note：SVDD1 is the power supply for IO(PB5-PB15)
SVDD2 is the power supply for IO(PA11-PA14, PE0, PE1, PB0, PB1)
SVDD3 is the power supply for IO(PG6-PG15)

1.2 Pin Description

Table1-1 AC5713A_QFN88 Pin Description

No.	Name	I/O type	Function	Other Function
1	PB12	I/O	GPIO	SENSORXD1: High-speed Sensor Data1 RMII_RX0_A: RMII Receive0(A) CAP3: Timer3 Capture ADC3: ADC Input Channel 3 SPI1_DOD(0): SPI1 Data Out(D)
2	PB11	I/O	GPIO	SENSORXD2: High-speed Sensor Data2 RMII_CRSDV_A: RMII Carrier Sense/Receive Valid(A) TMR1: Timer1 Clock In PWM3: Timer3 PWM Output SPI1_CLKD: SPI1 CLK(D)
3	PB10	I/O	GPIO	SENSORXD3: High-speed Sensor Data3 RMII_REFCLK_A: RMII Reference Clock (A) SPI2_DAT3B(3): SPI2 Data3(B) SD1_DAT1B: SD1 Data1(B)
4	PB9	I/O	GPIO	SENSORXD4: High-speed Sensor Data4 RMII_RXERR_A: RMII Receive Error(A) SPI2_CLKB: SPI2 CLK(B) SD1_DAT0B: SD1 Data0(B)
5	PB8	I/O	GPIO	SENSORXD5: High-speed Sensor Data5 RMII_TXEN_A: RMII Transmit Enable(A) SPI2_DOB(0): SPI2 Data Out(B) SD1_CLKB: SD1 CLK(B)
6	PB7	I/O	GPIO	SENSORXD6: High-speed Sensor Data6 RMII_TX1_A: RMII Transmit1(A) SPI2_DAT2B(2): SPI2 Data2(B) SD1_CMDB: SD1 CMD(B)
7	PB6	I/O	GPIO	SENSORXD7: High-speed Sensor Data7 RMII_TX0_A: RMII Transmit0(A) SPI2_DIB(1): SPI2 Data In(B) SD1_DAT3B: SD1 Data3(B)
8	PB5	I/O	GPIO	SENSORXCLK: High-speed Sensor Dlock CAP0: Timer0 Capture SPI2_CSB: SPI2 Chip Select(B) SD1_DAT2B: SD1 Data2(B)
9	SVDD1	P	IO Power1	——

No.	Name	I/O type	Function	Other Function
10	DRVREF	P	DDR REF	——
11	DRVDD	P	DDR Power	——
12	DRVDD	P	DDR Power	——
13	DVDD	P	Core Power	——
14	PE1	I/O	GPIO	SD0_DAT1D: SD0 Data1(D) UART3_RXA: UART3 Data In(A)
	PB1	I/O	GPIO	PWM0: Timer0 PWM Output IIC_SDA1_A: IIC Data1(A)
15	PE0	I/O	GPIO	SD0_DAT0D: SD0 Data0(D) UART3_TXA: UART3 Data Out(A)
	PB0	I/O	GPIO	ADC1: ADC Input Channel 1 IIC_SCL1_A: IIC SCLK(A)
16	SVDD2	P	IO Power2	——
17	PA14	I/O	GPIO	SD0_CLKD: SD0 Clock(D)
18	PA13	I/O	GPIO	SD0_CMDD: SD0 CMD(D)
19	PA12	I/O	GPIO	SD0_DAT3D: SD0 Data3(D)
20	PA11	I/O	GPIO	SD0_DAT2D: SD0 Data2(D)
21	USBVSS	P	USB Ground	——
22	USBVDD	P	USB Power	——
23	USB0DM	I/O	USB0DM	——
24	USB0DP	I/O	USB0DP	——
25	PR0	I/O	RTC I/O	PINR: PIN Reset
26	PR1	I/O	RTC I/O	ADC13: ADC Input Channel 13 PINR: PIN Reset
27	PR2	I/O	RTC I/O	ADC13: ADC Input Channel 13 PINR: PIN Reset(Default)
28	RTCOSCO	I/O	RTC OSCO	——
29	RTCOSCI	I/O	RTC OSCI	——
30	RTCVDD33	P	RTC Power	——
31	RTCVDD50	P	RTC Power	——
32	PA4	I/O	GPIO	SPI0_CLKA: SPI0 CLK(A)
33	PA3	I/O	GPIO	SPI0_DOA(0): SPI0 Data Out(A)
34	VDDIO	P	IO Power	——
35	PA1	I/O	GPIO	SPI0_DIA(1): SPI0 Data In(A)
36	PA0	I/O	GPIO	SPI0_CSA: SPI0 Chip Select(A)

No.	Name	I/O type	Function	Other Function
37	PH13	I/O	GPIO	UART0_RXC: Uart0 Data In(C) AVOUT: AV Output TMR3: Timer3 Clock In
	PH14	I/O	GPIO	ADC10: ADC Input Channel 10 CLKOUT1: Clock Out1 IIC_SDA0_B: IIC0 Data(B) Wakeup14: Port Wakeup 14
38	PH11	I/O	GPIO	AMUX1R: Simulator Channel 1 Right SD1_DAT0A: SD1 Data0(A) UART2_RXB: Uart2 Data In(B)
	PH12	I/O	GPIO	UART0_TXC: Uart0 Data Out(C) ADC9: ADC Input Channel 9 PWM2: Timer2 PWM output IIC_SCL0_B: IIC0 SCL(B)
39	PH10	I/O	GPIO	AMUX1L: Simulator Channel 1 Left SD1_CLKA: SD1 CLK(A) ADC12: ADC Input Channel 12 Wakeup13: Port Wakeup 13 UART2_TXB: Uart2 Data Out(B)
40	PH9	I/O	GPIO	MICR: MIC Right SD1_CMDA: SD1 CMD(A)
41	DACVDD	P	DAC Power	——
42	VCM	P	VCM	——
43	AVSSHP	P	HP Ground	——
44	DACL	O	DAC Left Channel	——
45	DACR	O	DAC Right Channel	——
	PH6	I/O	GPIO	MICL: MIC Left
46	AVDDHP	P	HP Power	——
47	PH5	I/O	GPIO	LCD_VSYNCAA: LCD Vertical Synchronization(group A) UART1_RXB: Uart1 Data In(B) MOTOR PWM_H3_B SD0_DAT1B: SD0 Data1(B)
48	PH4	I/O	GPIO	LCD_HSYNCAA: LCD Horizontal Synchronization(group A) EMI_RDAA: EMI Read(group A) MOTOR PWM_L3_B SD0_DAT0B: SD0 Data0(B)

No.	Name	I/O type	Function	Other Function
49	PH3	I/O	GPIO	LCD_DENAA: LCD Data Enable(group A) EMI_WRAA: EMI Write(group A) MOTOR PWM_H2_B SD0_CLKB: SD0 CLK(B)
50	PH2	I/O	GPIO	LCD_DCLKAA: LCD Data Clock(group A) UART1_TXB: Uart1 Data Out(B) MOTOR PWM_L2_B SD0_CMDB: SD0 CMD(B)
51	PH1	I/O	GPIO	LCD_DAT17A: LCD Data17(A) UART2_RXD: Uart2 Data In(D) TMR2: Timer2 Clock In MOTOR PWM_H1_B SD0_DAT3B: SD0 Data3(B)
52	PH0	I/O	GPIO	LCD_DAT16A: LCD Data16(A) UART2_TXD: Uart2 Data Out(D) SPI1_DIA(1): SPI1 Data In(A) CAP2: Timer2 Capture MOTOR PWM_L1_B SD0_DAT2B: SD0 Data2(B)
53	PE5	I/O	GPIO	ADC8: ADC Input Channel 8 IIC_SDA1_D: IIC1 Data(D) SPI1_DOA(0): SPI1 Data Out(A) Wakeup11: Port Wakeup 11 MOTOR PWM_H4_B
54	PE4	I/O	GPIO	IIC_SCL1_D: IIC1 SCL(D) SPI1_CLKA: SPI1 CLK(A) Wakeup10: Port Wakeup 10 MOTOR PWM_L4_B
55	DRVDD	P	DDR Power	——
56	DVDD	P	Core Power	——
57	SVDD3	P	IO Power3	——
58	PG15	I/O	GPIO	LCD_DAT15A: LCD Data15(A) EMI_D15A: EMI Data15(A) OSCO0 MOTOR PWM_H4_A
59	PG14	I/O	GPIO	LCD_DAT14A: LCD Data14(A) EMI_D14A: EMI Data14(A) OSCI0 MOTOR PWM_L4_A

No.	Name	I/O type	Function	Other Function
60	PG13	I/O	GPIO	LCD_DAT13A: LCD Data13(A) EMI_D13A: EMI Data13(A) MOTOR PWM_H3_A SD2_DAT1B: SD2 Data1(B) SPI2_DAT3A(3): SPI2 Data3(A)
61	PG12	I/O	GPIO	LCD_DAT12A: LCD Data12(A) EMI_D12A: EMI Data12(A) MOTOR PWM_L3_A SD2_DAT0B: SD2 Data0(B) SPI2_DAT2A(2): SPI2 Data2(A)
62	PG11	I/O	GPIO	LCD_DAT11A: LCD Data11(A) EMI_D11A: EMI Data11(A) MOTOR PWM_H2_A SD2_CLKB: SD2 CLK(B) SPI2_DIA(1): SPI2 Data In(A)
63	PG10	I/O	GPIO	LCD_DAT10A: LCD Data10(A) EMI_D10A: EMI Data10(A) MOTOR PWM_L2_A SD2_CMDB: SD2 CMD(B) SPI2_DOA(0): SPI2 Data Out(A)
64	PG9	I/O	GPIO	LCD_DAT9A: LCD Data9(A) EMI_D9A: EMI Data9(A) MOTOR PWM_H1_A SD2_DAT3B: SD2 Data3(B) SPI2_CLKA: SPI2 CLK(A)
65	PG8	I/O	GPIO	LCD_DAT8A: LCD Data8(A) EMI_D8A: EMI Data8(A) MOTOR PWM_L1_A SD2_DAT2B: SD2 Data2(B) SPI2_CSA: SPI2 Chip Select(A)
66	PG7	I/O	GPIO	LCD_DAT7A: LCD Data7(A) EMI_D7A: EMI Data7(A) UART0_RXB: Uart0 Data In(B) ADC7: ADC Input Channel 7 IIC_SDA0_A: IIC0 Data(A)
67	PG6	I/O	GPIO	UART0_TXB: Uart0 Data Out(B) IIC_SCL0_A: IIC0 SCLK(A)
68	DSI_D0N	O	MIPI DSI Lane	MIPI DSI data(0/1/) lane(P/N) MIPI DSI clock lane(P/N)
69	DSI_D0P	O	MIPI DSI Lane	MIPI DSI data(0/1/) lane(P/N) MIPI DSI clock lane(P/N)

No.	Name	I/O type	Function	Other Function
70	DSI_D1N	O	MIPI DSI Lane	MIPI DSI data(0/1/) lane(P/N) MIPI DSI clock lane(P/N)
71	DSI_D1P	O	MIPI DSI Lane	MIPI DSI data(0/1) lane(P/N) MIPI DSI clock lane(P/N)
72	DSI_D2N	O	MIPI DSI Lane	MIPI DSI data(0/1) lane(P/N) MIPI DSI clock lane(P/N)
73	DSI_D2P	O	MIPI DSI Lane	MIPI DSI data(0/1) lane(P/N) MIPI DSI clock lane(P/N)
74	MIPIAVDD12	P	MIPI AVDD	——
75	MIPIAVDD33	P	MIPI Power	——
76	CSI_D2N	I	MIPI CSI Lane	MIPI CSI data(0/1) lane(P/N) MIPI CSI clock lane(P/N)
77	CSI_D2P	I	MIPI CSI Lane	MIPI CSI data(0/1) lane(P/N) MIPI CSI clock lane(P/N)
78	CSI_D3N	I	MIPI CSI Lane	MIPI CSI data(0/1) lane(P/N) MIPI CSI clock lane(P/N)
79	CSI_D3P	I	MIPI CSI Lane	MIPI CSI data(0/1) lane(P/N) MIPI CSI clock lane(P/N)
80	CSI_D4N	I	MIPI CSI Lane	MIPI CSI data(0/1) lane(P/N) MIPI CSI clock lane(P/N)
81	CSI_D4P	I	MIPI CSI Lane	MIPI CSI data(0/1) lane(P/N) MIPI CSI clock lane(P/N)
82	PE2	I/O	GPIO	VPP CLKOUT0: Clock Out0 PWM4: Timer4 PWM Output
83	VDD28	P	VDD28	——
84	VDDIO	P	IO Power	——
85	AVDDR	P	Power	——
86	VDD15	P	VDD15	——
	PB15	I/O	GPIO	UART0_RXD: Uart0 Data In(D) OSCO1 CAP1: Timer1 Capture
87	PB14	I/O	GPIO	UART0_TXD: Uart0 Data Out(D) OSCI1 TMR0: Timer0 Clock In ADC4: ADC Input Channel 4 Wakeup9: Port Wakeup 9

No.	Name	I/O type	Function	Other Function
88	PB13	I/O	GPIO	SENSORXD0: high-speed sensor data0 RMII_RX1_A: RMII Receive1(A) PWM1: Timer1 PWM Output SPI1_DID(1): SPI1 Data In(D)

(★Note: 1. P----Power Supply 2. I----Input 3. O----Output 4. I/O----Bi-direction)

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Item	Range	Unit	Remarks
SVDD1/SVDD2/SVDD3	Special IO Logic Voltage	-0.3 to 3.6	V	---
VDDIO/USBVDD /MIPIAVDD33	Digital Voltage	-0.3 to 3.6	V	---
AVDDHP	Analog Voltage	-0.3 to 3.6	V	---
DVDD/MIPIAVDD12	Core Voltage	-0.3 to 1.3	V	---
DRVDD	DDR1 Voltage	-0.3 to 2.7	V	---
AVDDR	Digital Voltage	-0.3 to 3.3	V	---
RTCVDD50	RTC Voltage	-0.3 to 5.5	V	---
V_{IO1}	Voltage applied on normal pin	-0.3 to VDDIO+0.3	V	Relative to ground
V_{IO2}	Voltage applied on special pin	-0.3 to SVDD1/2/3+0.3	V	Relative to ground
T_{OPE}	Operating Temperature	-40 to 85	℃	---
T_{STG}	Storage Temperature	-65 to 150	℃	---

2.2 Recommended Operating Conditions

Table 2-2

Symbol	Item	Min	Typ	Max	Unit
SVDD1/SVDD2/SVDD3	1.8V Logic Voltage	1.7	1.8	1.9	V
	3.3V Logic Voltage	3.0	3.3	3.6	V
VDDIO/USBVDD /MIPIAVDD33	Digital Voltage	3.0	3.3	3.6	V
AVDDHP	Analog Voltage	3.0	3.3	3.6	V
DVDD/MIPIAVDD12	Core Voltage	1.0	1.1	1.2	V
DRVDD	DDR1 Voltage	2.3	2.5	2.7	V
AVDDR	Digital Voltage	1.7	2.5	2.7	V
RTCVDD50	RTC Voltage	2.8	4.2	5.5	V

2.3 IO Input/Output Electrical Characteristics

Table 2-3

Input Characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low (logic 0) voltage	-0.3	-	0.3* VDDIO	V	VDDIO = 3.3V
V_{IH}	Input high (logic 1) voltage	0.7* VDDIO	-	VDDIO+0.3	V	VDDIO = 3.3V
Output Characteristics						
V_{OL}	Output low (logic 0) voltage	-	-	0.1* VDDIO	V	VDDIO = 3.3V
V_{OH}	Output high (logic 1) voltage	0.9* VDDIO	-	-	V	VDDIO = 3.3V

2.4 IO Output Drive Strength Pull Up/Down Characteristics

Table 2-4

Port	Drive Strength	Pull Up Resistance	Pull Down Resistance	Note
PA0,PA1 PA3,PA4 PA11-PA14 PB0,PB1 PB5-PB15 PG0 - PG15 PH0-PH6 PH9-PH14	Strong drive: 16mA / 21mA Weak drive: 2mA / 7mA	10K	10K	Test Conditions: VDDIO = 3.3V SVDD1 = 3.3V SVDD2 = 3.3V SVDD3 = 3.3V
PE0-PE2,PE4,PE5	7mA	10K	10K	---
PR0 -PR2	Strong drive: 16mA / 21mA Weak drive: 2mA / 7mA	10K	10K	Supplied by RTC power
USB_DP	10mA	1.5K	15K	Use as normal IO
USB_DM	10mA	---	15K	Use as normal IO

(★NOTE: precision of pull-up and pull-down resistor is ±20%)

2.5 LDO Characteristics

Table 2-5

Internal LDO	Output Voltage Range	Drive Stength	Test Conditions
VDD15	1.3V-2.0V	~50 mA	AVDDR=2.5V
VDD28	2.5V-3.2V	~100 mA	VDDIO=3.3V

2.6 Audio DAC Characteristics

Table 2-6

Symbol	Parameters	Min	Typ	Max	Unit	Test Conditions
SNR	Signal to Noise Ratio	-	95	-	dB	1KHz, SR=44.1K, Mute File, CR=192Kbps
THD+N	Total Harmonic Distortion + Noise	-	-73	-	dB	(-1.5dB) 1KHz, SR=44.1K, CR=192Kbps

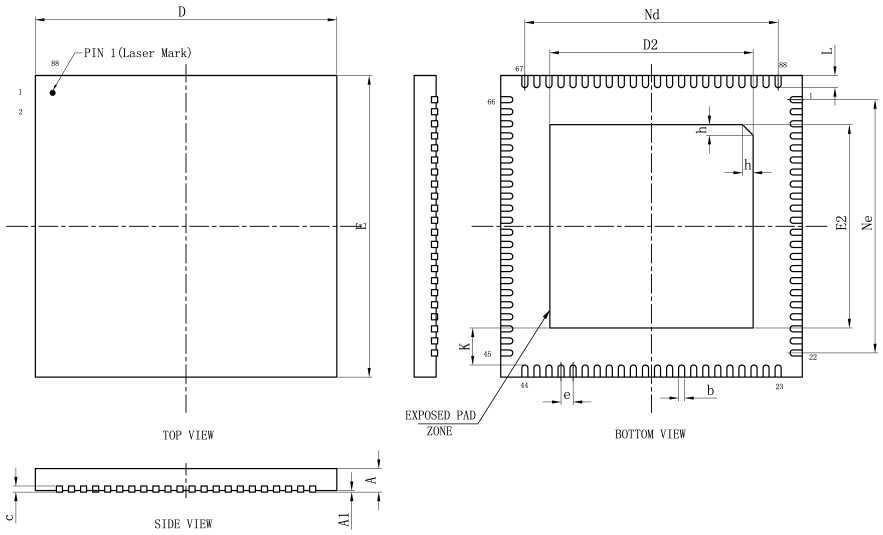
2.7 Audio ADC Characteristics

Table 2-7

Symbol	Parameters	Min	Typ	Max	Unit	Test Conditions
SNR	Signal to Noise Ratio	-	85	-	dB	1KHz, SR=44.1K, Mute File, CR=192Kbps
THD+N	Total Harmonic Distortion + Noise	-	-75	-	dB	(-1.5dB) 1KHz, SR=44.1K, CR=192Kbps

3. Package

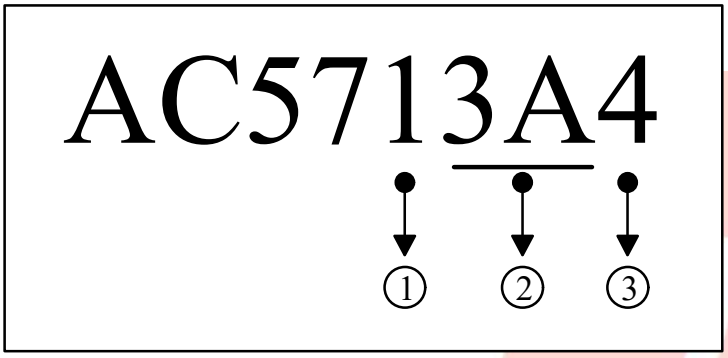
3.1 QFN_88PIN Package Diagram



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	9.90	10.00	10.10
D2	6.64	6.74	6.84
e	0.40BSC		
Nd	8.40REF		
E	9.90	10.00	10.10
E2	6.64	6.74	6.84
Ne	8.40REF		
L	0.30	0.40	0.50
K	0.20	-	-
h	0.30	0.35	0.40
L/F载体尺寸 (mil)	300x300		

Figure 3-1 AC5713A_QFN88 Package Diagram

4. Package Type Specification



① 0 represents DDR2 and 1 represents DDR1

② Different numbers and letters represent different packages

③ Represents the sdram size of the chip, 8 represents 512M, 4 represents 256M, 2 represents 128M and 1 represents 64M.

5. Version Information

Date	Version Number	Description
2021.07.28	V1.0	Initial draft