NOVATEK 聯詠科技

Data Sheet

NT96675M

Imaging Processor

Preliminary

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Revision History

Rev.	Date	Author	Contents
V0.1	2017/07/25	Kevin Hung	draft
V0.2	2017/09/25	Kevin Hung	Modify electrical specification / HSI pin mux table
V0.3	2017/11/06	Kevin Hung	Modify part number and electrical specification

Features

■ High Performance 32-bit CPU

- □ Dual MIPS32 24Kec with ASE DSP extension
- □ MMU embedded
- □ CPU1 with 16KB instruction and 16KB data cache
- □ CPU2 with 32KB instruction and 32KB data cache
- □ CPU operating frequency up to 640MHz
- □ Embedded ICE makes firmware debugging easier

■ High Performance CEVA MM3101 Image/Video DSP

- □ 540 MHz CEVA DSP

■ Power Management features

- □ Firmware configurable operating frequency of each functional block to meet best power budget
- □ Internal power domain partition

■ Integrated Clock Generator

- □ Internal PLL with spread spectrum capability
- □ 12MHz system
- □ 32768Hz RTC oscillator

■ Scalable Memory Bus Architecture

- □ 16-bit DDR3/3L/2L SDRAM bus, supporting up to 8Gb
- □ DRAM operating data rate up to DDR3-1600, DDR3L-1400 or DDR2L-1066 without ODT
- □ SIP DDR3 1Gb DRAM

□ Sensor Interface Engine

- □ Support high speed serial interface like MIPI(1.5G)/ sub-LVDS /HiSPi(1G) up to 4 channels and 2 clocks for most commercial CMOS sensors including Sony, Panasonic, Aptina, Samsung, Sharp and Omnivision, etc. 2 clock channels allow dual two data lanes sensors application usage.
- □ Support parallel sensor interface for most commercial CMOS sensors including Aptina and Omnivision
- □ Support max. 1 BT.601/656(8-bit)/BT.1120 video input
- □ Support 8-/10-/12-bit sensor data input
- □ Support burst shot up to 30fps for 5MP sensor
- □ Support parallel interface sensor pixel clock up to 120MHz
- □ Support RGBIR 4x4
- □ Support HDR sensor composition such as SONY DOL mode and Omnivision staggered mode

- Built-in color pattern generation
- Sensor black level clamping
- Efficient defect concealment algorithm
- Raw image scale down for video & high ISO image
- Flexible image analysis flow for AE, AWB and AF purpose
- Programmable histogram analysis
- R/G/B Gamma LUT for sensor linearization correction

Image Processing Engine

- In-pipeline lens shading compensation technology
- In-pipeline color shading compensation technology
- Support in-frame dark frame subtraction with smart defect detection algorithm
- Support EIS with gyro-sensor input
- Mechanical shutter control
- Flash light control
- Advanced image pipeline architecture for multi-purpose hardware acceleration
- Proprietary advanced anti-alias Bayer CFA color interpolation
- Advanced edge rendering control and continuity enhancement
- Powerful noise reduction technology for still and video recording
- Support advanced motion compensated temporal filtering (MCTF) for efficient video noise reduction
- Support temporal noise reduction with ghost reduction
- R/G/B Gamma LUT
- High precision color correction matrix for sRGB or specific color requirement
- Brightness/contrast and hue/saturation adjustment
- Specific color control technology (Patented)
- False color suppression
- Anti-fog function
- Wide dynamic range (WDR) for global/local illumination enhancement

Image Manipulation Engine

- High quality scaling engine for seamless digital zooming from 1/16x to 16x
- Support thumbnail image generation
- Forward/inverse color space transform

Face Detection Engine

- Very high speed face detection and tracking

- High accuracy under different light source
- Programmable target data base

Digital Image Stabilizer

- Remove unintended hand movement from an image sequence
- Single frame compensation for video (Total compensation)
- Accumulate frame compensation for video (Smart compensation)
- Programmable total compensation range

LCD/TV Display

- High performance scaling up/down engine, programmable gamma correction, color transform and color management for LCD or TV display
- Separate OSD for LCD panel and TV
- Support digital LCD interface for AUO, Casio, CMI (all digital panels will be supported)
- Support 90° rotation/flip/mirror
- Support PAL / NTSC video encoder (CVBS format) with automatic load detection
- Integrated 1 internal 10-bit video DACs
- Support digital interface BT.601/656/1120 output port
- 3.3V / 1.8V LCD / Digital video out

Graphic Engine

- Copy and paste
- Geometric operation including mirror, flip and rotation
- Arithmetic operation including addition, subtraction, color keying, logic operation and alpha blending

Cipher

- 64-bit DES, 3DES support
- Supports 3-key and 2-key modes for the 3DES algorithm
- AES-128 and AES-256
- Supports the operating modes of counter with Cipher Block Chaining-Message Authentication Code (CCM), Galois/Counter Mode (GCM), electronic code book (ECB), cipher block chaining (CBC), cipher feedback (CFB), output feedback (OFB), and counter (CTR) for the DES/3DES/AES algorithm
- Support multi-channel encryption and decryption

Hash

- Support SHA1,SHA256,HMAC-SHA1,HMAC-SHA256 algorithm

RSA

- Support 512-bit, 1024-bit, 2048-bit , 4096-bit key
- Support Key checksum by CRC32

True Random Number Generator

- Generate true random number
- 32-bits Random number generator

Video CODEC

- Support H.264/AVC codec BP/MP/HP, level 5.1
- Support H.265/HEVC codec MP, level 5.0
- Support real-time capability for 3-megapixel@30fps +720p@30fps + WVGA@30fps
- Support frame rotation 90 degree counterclockwise and clockwise
- Support configurable GOP
- Support ROI (10 sets) enhancing picture quality
- Support CBR, VBR and Macro block QP table
- Support OSD function
- Support Scalable Video Codec (SVC-T)
- Support video format MP4, AVI, MOV
- Support full frame still capture while video recording

F/W Audio CODEC

- AAC encode / decode (32KHz, 48KHz @ 192kbps)
- ADPCM /G.711 / G.726
- AEC / ANR and ALC

H/W Audio CODEC

- stereo 16-bits ADC audio recording
- stereo 16-bits DAC audio playback
- Programmable ALC / Noise Gate l
- Audio sampling rate : 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48kHz
- Support dual microphone inputs

JPEG CODEC

- Supports Motion JPEG 30fps@1080P30 video clip/playback function
- Max. pixel clock 240Mpixel / sec
- Support ISO/IEC 10918-1 baseline JPEG compression/decompression.
- Still image maximum resolutions will be up to 65536x65536 pixels
- Support input format: 422, 420, 411, 400, 211
- JPEG supports downloadable Quantization and Huffman tables

- Support Exchangeable Image File format (EXIF 2.2.3 and newer)
- Support MPO file format for 3D image

Digital Audio Interface

- Support I2S codec interface
- Audio clock generator

Dual Graphic-based OSD

- Support 8-bit palette and ARGB(8565 or 8888) OSD architecture
- 256 colors simultaneously out of true color at 8-bit palette OSD
- Programmable width & height to meet LCD/TV's resolution exactly
- Picture in picture function
- Support Codec video encode OSD function
- 8 sets privacy mask
- Support 4 sets data stamp

Storage Memory Controller

- Secure Digital card and SDIO
- Support SD 3.0
- Support UHS-I: UHS50, UHS104 (Max. freq. 96MHz)
- Support SPI-NAND and SPI-NOR flash
- Support eMMC v5.0 interface

USB

- Fully compliant with USB2.0 device/host (1 set)
- Support Control / Isochronous / Interrupt and Bulk transfer
- Support PC camera mode

Timers

- RTC can be powered by separate backup battery and operating from 1.5V to 3.3V
- Watch dog timer
- 20 programmable HW timers support resolution up to 3MHz and 32 bits counter

Peripheral Interface

- Support I2C interface
- Support 16 channels PWM including built-in 4 (3 sets) pattern generators for µ-Stepping motor control
- Support GPIO and flexible PWM interface with micro-stepping
- Support programmable 3-wired serial interface
- Support SPI interface

- Dedicated SPI for gyroscope reading
- Support NFC & BLE4.0 interface
- Support UART interface
- Support Remote interface
- Support 4 channels of 10-bit ADC, the max. sample rate up to 12.5 KHz per channel
- Embed Ethernet 10M/100M MAC and support RMII/MII/RevMII interface. PHY clock output and TSO/UFO acceleration.
- Embedded Ethernet PHY, Fully compliant with 100BASE-TX, and 10BASE-T PMD level standards (IEEE 802.3, 802.3u)

On-chip Boot Strap Loader

- Built-in on-chip mask ROM
- User program can be stored in NAND-type flash and external static memory is not necessary
- On-chip mask ROM can be disabled
- System can boot from SPI NOR/ NAND flash, memory cards, eMMC, Ethernet

Quadruple Voltage Power Supply

- 0.9V core logic voltage
- 1.5V DDR3, 1.35V DDR3L or 1.5V DDR2L SDRAM interface voltage
- 2.5V analog circuit voltage
- 3.3V I/O interface and analog circuit voltage

Package

- NT96675MBG: 280 ball TFBGA, 12x12 mm^2

General Description

NT96675M is a highly-integrated SoC targets on dash-cam, battery cam system. It builds in MIPS32 24KEc dual cores CPU, video input, ISP, H.264/H265 encoder, JPEG encoder, intelligent video analysis functions, graphic engine, display controller, encryption engine, ethernet PHY, USB 2.0 Host/Device, RTC, SD/SDIO 3.0 and built-in DDR2L/DDR3 SDRAM to reduce the overall system cost.

Block Diagram